App. No. 09/700,940
Office Action Dated February 1, 2005

REMARKS

Favorable reconsideration of this application is requested in view of the above amendments and the following remarks. Claims 1 and 6 are amended editorially.

Claims 1, 2, 4, and 6 were rejected as being unpatentable over Kinoshita (US 5,869,852) in view of Miki (US 5,761,076). Applicants traverse this rejection. Claims 1 and 6 recite that a capacitance value of a power supply capacitor cell is determined based on a drive load capacity value of a logic gate cell. The power supply capacitor cell (with the determined value) is arranged in the vicinity of the logic gate cell on which its value was based. The rejection concedes that Kinoshita fails to suggest that a capacitance value of the power supply capacitor cell is determined using a drive load capacity value of the logic gate cell. Similarly, Miki does not suggest calculating a capacitance value of the power supply capacitor cell **prior** to arrangement of layout of the standard cells, i.e. locating the power supply capacitor cell in the vicinity of or adjacent to the logic gate cell used to determine the capacitance value, as required by claims 1 and 6. Rather, Miki discloses a capacitance calculation based on post-layout standard cell wiring (see column 1, lines 29-32 and column 4, lines 46-54). The calculation taught by Miki would be ineffective if calculated prior to layout of the standard cells, as the goal of Miki is to perform post-layout timing analysis.

Further, the "capacitance element" disclosed by Miki is referring to an equivalent circuit for representing the capacitance of post-layout wiring (see column 1, lines 23-24). Calculation of this equivalent circuit value is not equivalent to calculating a capacitance value of the power supply capacitor cell, as required by claims 1 and 6.

Even further, claim 4 requires that the power supply capacitor cell is arranged in spaces where standard cells are not placed by automatic arrangement wiring. In contrast, Kinoshita teaches placing capacitor cells (62) at **all** wiring channels (see column 15, lines 1-11 and Figure 29). The method of Kinoshita would result in a costly increase of total die area. In the present invention, the capacitor cells are only arranged in dead space or spaces not utilized by the automatic arrangement of the standard cells.

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Favorable reconsideration of claims 1, 2, 4, and 6 is requested.

Claim 3 was rejected as being unpatentable over Kinoshita, in view of Miki, and further in view of Eto (US 6,229,363). Applicants traverse this rejection. Eto does not remedy the deficiencies of Kinoshita and Miki, as previously noted. Applicants are not conceding the correctness of the rejection as applied to claim 3. Favorable reconsideration of claim 3 is requested.

In view of the above, favorable reconsideration in the form of a notice of allowance is requested. Any questions regarding this communication can be directed to the undersigned attorney, Douglas P. Mueller, Reg. No. 30,300, at (612)455-3804.

Respectfully submitted,

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